Performance analysis of a symbol slicing majority vote combining receiver for binary optical heterodyne ASK with phase-noise-optimised decision thresholds

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Abstract: The performance of a binary optical heterodyne ASK receiver in the presence of photo-detector shot noise and laser phase noise has been investigated. To reduce the effects of phase noise on the receiver error rate, the maximum likelihood approach is used to optimise the decision threshold on the basis of the severity of phase noise indicated by the laser linewidth. It is assumed that the receiver uses symbol slicing and majority vote decision combining. Threshold optimisation is applied to each slice (chip) of the received bit duration. It is found that the receiver performance can be significantly improved by threshold optimisation. Majority voting is also found to improve the receiver performance for a wide range of signal-to-noise ratio values.

1 Introduction

The performance of heterodyne optical communication receivers can be significantly degraded by semiconductor laser phase noise [1–4]. Existing heterodyne receivers are mostly based on matched filter models (or equivalently, correlators or integrate-and-dump filters) which are known to be optimal in additive white Gaussian noise (AWGN), that is in the absence of laser phase noise [5]. A brief literature review of optical receiver performance in the presence of phase noise can be found in Banat and Awad [6].

We investigate the performance of a binary optical heterodyne ASK receiver in the presence of photodetector (PD) shot noise (this noise is available at the electrical output of the PD, and hence, is different from additive optical noise that may be added by an optical preamplifier) and laser phase noise. PD shot noise is known to be AWGN. Therefore receiver optimisation against this kind of noise follows conventional matched filter models vastly used in the literature. However, laser phase noise is not AWGN. In fact, it is not even additive. The maximum a posteriori approach cannot be directly applied to the design of phase-noise-optimum receivers because of mathematical intractability. This is the main reason why most existing literature related to receiver optimisation starts with a matched filter model. In many cases, this model is even used without any modification. When we start with a matched filter-based receiver, the phase noise effect manifests itself in the form of a random multiplicative noise which has no analytical probability density function [7–9].

In an earlier work, Banat and Awad [6] introduced the use of symbol slicing and majority vote combining to a binary non-coherent FSK receiver in an attempt to improve the system performance in the presence of laser phase noise.

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The proposed receiver in Banat and Awad [6] was found to perform better than the receivers based on whole symbol decisions. Symbol slicing and majority vote combining will be used in this paper in a binary coherent ASK receiver, which is usually severely affected by laser phase noise.

To reduce the effects of phase noise on the receiver error rate, we use the maximum likelihood approach to optimise the decision threshold based on the severity of phase noise measured by the laser linewidth. The receiver uses symbol slicing and majority vote decision combining. In this configuration, the received symbol duration T is split into L chips each of duration $T_c = T/L$. A binary decision is made on each chip. On the basis of the chip decisions, a symbol decision is made in favour of the symbol with a majority of chip decisions in its favour. Threshold optimisation is applied to each slice (chip) of the received bit duration. It is found that the receiver performance can be significantly improved by threshold optimisation. Majority voting is also found to improve the receiver performance for a wide range of signal-to-noise ratio values.

2 System model

In a binary ASK system, the transmitted signal can be written in the form

$$s(t) = \begin{cases} s_1(t) = A_s \cos[2\pi f_s t + \theta_s(t)], & \text{‘1’} \\ s_0(t) = 0, & \text{‘0’} \end{cases} \tag{1}$$

where A_s is the signal amplitude, assumed to be constant, f_s is the optical carrier frequency and $\theta_s(t)$ is a Wiener–Levy laser phase noise process, having a linewidth equal to β_s. A heterodyne receiver first adds the incoming signal $s(t)$ to a locally-generated signal $s_{lo}(t)$ then applies the sum signal to a PD, which produces a current $i(t)$. This process is illustrated in Fig. 1. The local signal will be assumed to have the form

$$s_{lo}(t) = A_{lo} \cos[2\pi f_{lo} t + \theta_{lo}(t)] \tag{2}$$

where A_{lo} and f_{lo} are the local laser signal amplitude and frequency, respectively, while $\theta_{lo}(t)$ is its phase noise process, assumed to be Wiener–Levy with linewidth β_{lo}. Phase

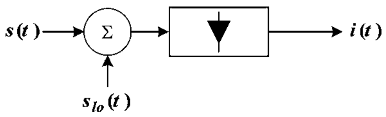

Fig. 1 *Heterodyne detector*

noise processes $\theta_s(t)$ and $\theta_{lo}(t)$ will be assumed to be representable in the form

$$\theta(t) = 2\pi \int_0^t \zeta(\tau)\mathrm{d}\tau \tag{3}$$

where $\zeta(t)$ is a zero-mean white Gaussian random process with double-sided power spectral density $\beta_s/2\pi$ for $\theta_s(t)$, and $\beta_{lo}/2\pi$ for $\theta_{lo}(t)$.

Without loss of generality, we'll ignore the proportionality constants involved in the PD optical-to-electrical conversion process. Hence, the PD output current will be given by

$$\begin{aligned} i(t) &= \mathrm{LP}\{|s(t) + s_{lo}(t)|^2\} + x(t) \\ &= \begin{cases} i_1(t), & \text{when a '1' is transmitted} \\ i_0(t), & \text{when a '0' is transmitted} \end{cases} \end{aligned} \tag{4}$$

where LP(·) denotes the familiar low pass operator. If a '1' is transmitted the PD current is given by

$$\begin{aligned} i_1(t) &= \mathrm{LP}\{|s_1(t) + s_{lo}(t)|^2\} + x_1(t) \\ &= I_{dc,1} + A_{lo}A_s \cos[2\pi f_h t + \theta_h(t)] + x_1(t) \end{aligned} \tag{5}$$

where

$$I_{dc,1} = \frac{A_s^2 + A_{lo}^2}{2} \tag{6}$$

and f_h is the heterodyne frequency given by

$$f_h = f_{lo} - f_s \tag{7}$$

$\theta_h(t) = \theta_{lo}(t) - \theta_s(t)$ will be termed the heterodyne phase noise. Owing to the statistical independence of $\theta_s(t)$ and $\theta_{lo}(t)$, it can be easily shown that $\theta_h(t)$ satisfies (3) with a linewidth equal $\beta = \beta_{lo} + \beta_s$. The PD shot noise current $x_1(t)$ is AWGN with power spectral density [4] equal to $A_{lo}^2/2$.

When a '0' is transmitted the PD current is given by

$$\begin{aligned} i_0(t) &= \mathrm{LP}\{|s_{lo}(t)|^2\} + x_0(t) \\ &= I_{dc,0} + x_0(t) \end{aligned} \tag{8}$$

where

$$I_{dc,0} = \frac{A_{lo}^2}{2} \tag{9}$$

and $x_0(t)$ is AWGN with power spectral density [4] equal to $A_{lo}^2/2$. The symbol slicing receiver performs a matched filtering operation on each chip, as shown in Fig. 2. The result is the chip decision variable V_k. This process is

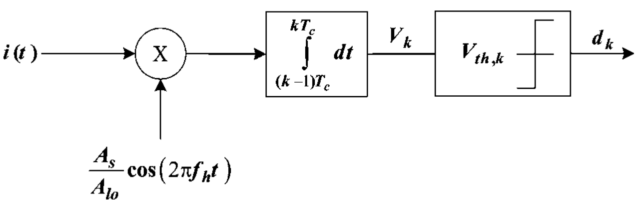

Fig. 2 *Chip decision circuit*

repeated for all $k = 1, 2, \ldots, L$. Each decision variable is then compared to a threshold $V_{th,k}$ to make a chip decision d_k. The chip decisions are made according to the rule

$$V_k \underset{\text{'0'}}{\overset{\text{'1'}}{\gtrless}} V_{th,k} \tag{10}$$

Chip decision thresholds $\{V_{th,k}\}$ will be derived so that chip decisions are optimum in the maximum likelihood sense. Note that effects like pulse shaping, time jitter and eye closure are not taken into account. Would such effects be considered, chip error rate performance would naturally tend to deteriorate. Once all L chip decisions have been made, a symbol decision is made in favour of the symbol with more chip decision in its favour. That means, for example, that '1' is decided if at least $(L+1)/2$ '1' chip decisions have been made. Note that, to avoid cases of indecision, L will always be chosen to be odd.

The chip decision variable V_k can be easily found to be equal to

$$V_k = \begin{cases} m_c\eta_k + X_{1,k}, & \text{'1'} \\ X_{0,k}, & \text{'0'} \end{cases} \tag{11}$$

where m_c is the chip energy and η_k is a filtered phase noise random variable. m_c and η_k are given by

$$m_c = \frac{A_s^2 T_c}{2} \tag{12}$$

$$\eta_k = \frac{1}{T_c}\int_{(k-1)T_c}^{kT_c} \cos[\theta_h(t)]\,\mathrm{d}t \tag{13}$$

The noise output of the PD is given by

$$X_{l,k} = \frac{A_s}{A_{lo}}\int_{(k-1)T_c}^{kT_c} x_l(t)\cos(2\pi f_h t)\,\mathrm{d}t, \quad l = 0, 1 \tag{14}$$

It can be easily shown that $X_{l,k}$ has a variance $\sigma^2 = m_c/2$ for $l = 0, 1$.

3 Error probability derivations

To determine the bit error probability we first use the total probability theorem to find the chip probability of error, that is

$$P_k(e) = \frac{1}{2}[P_k(e/1) + P_k(e/0)] \tag{15}$$

where $P_k(e/1)$ and $P_k(e/0)$ are used to denote chip error probabilities conditioned on the transmission of a '1' or '0', respectively. After the chip decisions are made, a bit decision is made based on majority voting. A bit error occurs if a majority of chip decisions are wrong, that is

$$P(e) = \sum_{l=(L+1)/2}^{L} \binom{L}{l} (P_k(e))^l (1 - P_k(e))^{L-l} \tag{16}$$

Note that owing to the unavailability of analytical PDF's of $\{\eta_k\}$, we will need to initially find chip error probabilities $P_k(e/\eta)$ that are conditional on $\{\eta_k\}$. This is done through a slight modification to (15) that takes into account the conditioning on $\{\eta_k\}$ that is

$$P_k(e|\eta) = \frac{1}{2}[P_k(e/1, \eta) + P_k(e/0, \eta)] \tag{17}$$

Then, by means of a similar modification to (16), the conditional bit error probability $P(e/\eta)$ is found according to

$$P(e/\eta) = \sum_{l=(L+1)/2}^{L} \binom{L}{l} [P_k(e/\eta)]^l [1 - P_k(e/\eta)]^{L-l} \quad (18)$$

The unconditional bit error probability is found by numerically averaging $P(e/\eta)$ over the phase noise random variables $\{\eta_k\}$.

3.1 Probability of error with no threshold optimisation

To appreciate the performance advantage gained by threshold optimisation we will start by assuming that no such optimisation has been applied, so that $V_{th} = m_c/2$ (this is what is usually done when phase noise is not present)

$$P_k(e/\eta) = \frac{1}{2}\left[\Pr\left\{m_c\eta_k + X_{1,k} < \frac{m_c}{2}\right\} + \Pr\left\{X_{0,k} > \frac{m_c}{2}\right\}\right] \quad (19)$$

The last result can be easily translated into

$$P_k(e/\eta) = \frac{1}{2}\left[\Pr\left\{X_{1,k} > (2\eta_k - 1)\frac{m_c}{2}\right\} + \Pr\left\{X_{0,k} > \frac{m_c}{2}\right\}\right] \quad (20)$$

which finally results in

$$P_k(e|\eta) = \frac{1}{2}\left[Q\left((2\eta_k - 1)\sqrt{\frac{m_c}{2}}\right) + Q\left(\sqrt{\frac{m_c}{2}}\right)\right] \quad (21)$$

where $Q(\cdot)$ is the well known Q function, defined by

$$Q(x) = \frac{1}{\sqrt{2\pi}}\int_x^{\infty} e^{-u^2/2}\,du \quad (22)$$

3.2 Probability of error with threshold optimisation

Let us now set the chip decision thresholds to

$$V_{th,k} = \alpha_k \frac{m_c}{2} \quad (23)$$

where $\{\alpha_k\}$ are a group of positive constants that will be referred to as the threshold scale factors. With this modification, the chip error probabilities given in (19) are replaced by

$$P_k(e/\eta) = \frac{1}{2}\left[\Pr\left\{m_c\eta_k + X_{1,k} < \alpha_k\frac{m_c}{2}\right\} + \Pr\left\{X_{0,k} > \alpha_k\frac{m_c}{2}\right\}\right] \quad (24)$$

which leads to

$$P_k(e|\eta) = \frac{1}{2}\left[Q\left((2\eta_k - \alpha_k)\sqrt{\frac{m_c}{2}}\right) + Q\left(\alpha_k\sqrt{\frac{m_c}{2}}\right)\right] \quad (25)$$

Making use of the fact that

$$\frac{d}{dx}Q(x) = -\frac{1}{\sqrt{2\pi}}e^{-x^2/2} \quad (26)$$

we can write

$$\frac{d}{d\alpha_k}P_k(e|\eta) = \frac{-1}{2\sqrt{2\pi}}\left[-\sqrt{\frac{m_c}{2}}e^{-m_c(2\eta_k-\alpha_k)^2/4} + \sqrt{\frac{m_c}{2}}e^{-m_c\alpha_k^2/4}\right] \quad (27)$$

Equating to zero and taking the expected value over η_k yields

$$E[e^{-m_c\eta_k(\eta_k-\alpha_k)}] = 1 \quad (28)$$

4 Results

Let us begin by defining the linewidth duration product (LDP) as the product of the heterodyne phase noise linewidth $\beta = \beta_{lo} + \beta_s$ and the bit duration T. Larger values of the LDP indicate more severe phase noise. We first studied the behaviour of the optimum threshold scale factors $\{\alpha_k\}$ as function of m, the received energy per bit. Fig. 3 shows this behaviour when $L = 1$. As can be clearly seen from this figure, the scale factor becomes smaller as the LDP increases. Hence, the need for threshold

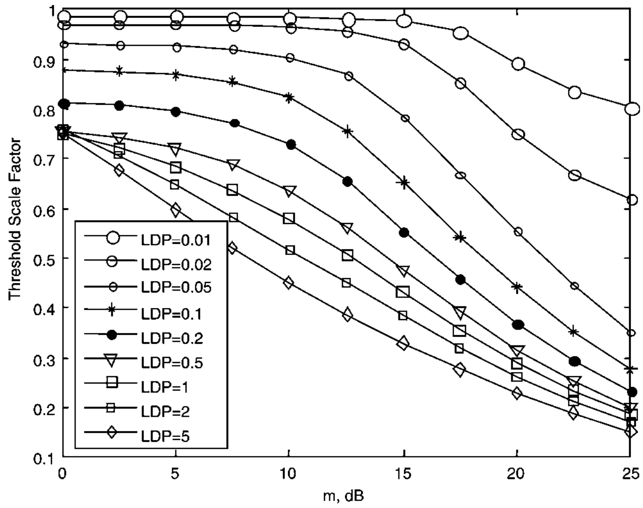

Fig. 3 *Optimum threshold scale factor α as function of m when L = 1*

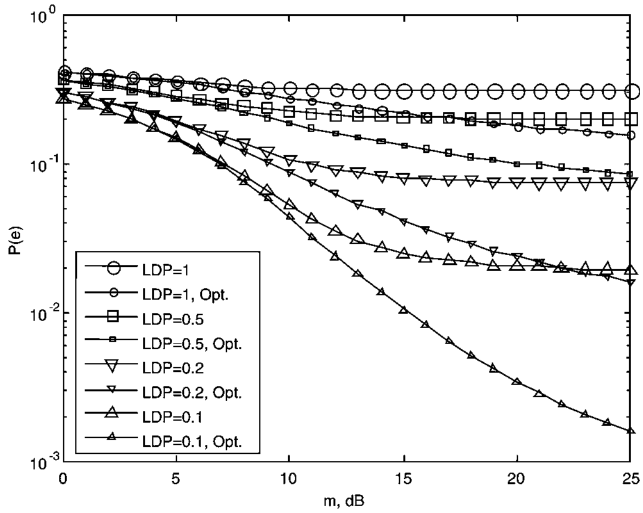

Fig. 4 *Bit error probability with and without threshold optimisation for the moderate phase noise case*

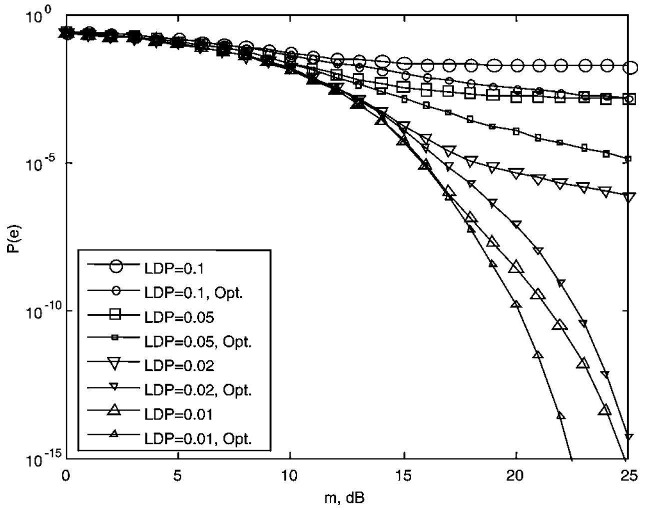

Fig. 5 *Bit error probability with and without threshold optimisation for the small phase noise case*

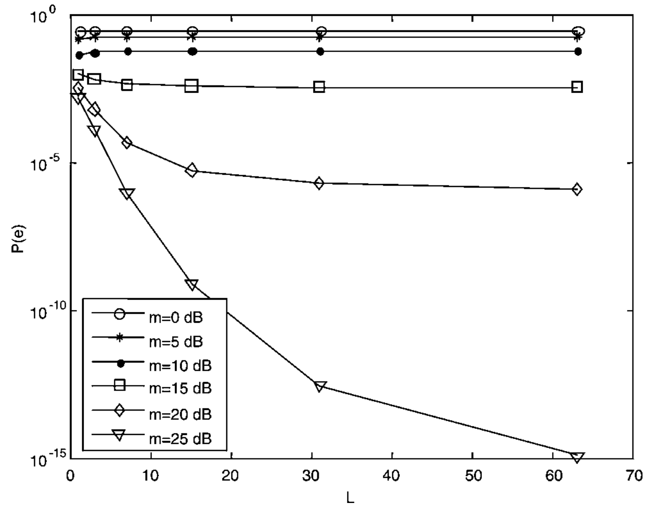

Fig. 8 *Bit error probability as function of the number of chips per bit (LDP = 0.1)*

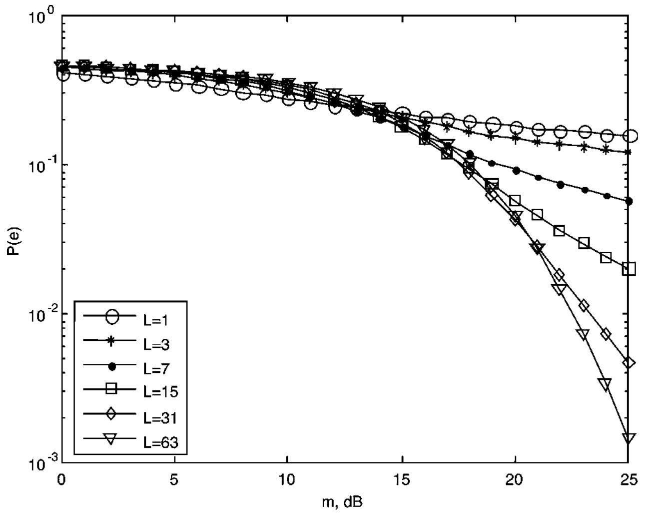

Fig. 6 *Bit error probability with threshold optimisation and majority vote combining for the moderate phase noise case*

optimisation is more pronounced when phase noise is stronger.

The effect of threshold optimisation on the bit error rate performance is illustrated by Figs. 4 and 5 for the cases of moderate ($0.1 \leq \text{LDP} \leq 1$) and small ($0.01 \leq \text{LDP} \leq 0.1$) phase noise, respectively. Significant bit error rate improvements can be seen, especially at larger values of m. Note that in the no threshold optimisation curves, the error rate reaches certain floors as m is increased beyond some values. This floor effect is drastically reduced by threshold optimisation, as clarified by Figs. 4 and 5.

Figs. 6 and 7 illustrate the bit error rate improvements achieved by the use of majority vote combining. Fig. 6 shows a moderate phase noise case (LDP = 1), and Fig. 7 shows a small phase noise case (LDP = 0.1).

The effect of increasing L, the number of chips per bit, on the error rate performance is shown in Fig. 8. It can be easily seen that L needs not be increased indefinitely. Actually, for each value of m there is a value beyond which increasing L presents too little error rate improvement to justify the resulting receiver complexity increase. Error rate floors as L becomes large are shown in Fig. 9 for several values of the LDP.

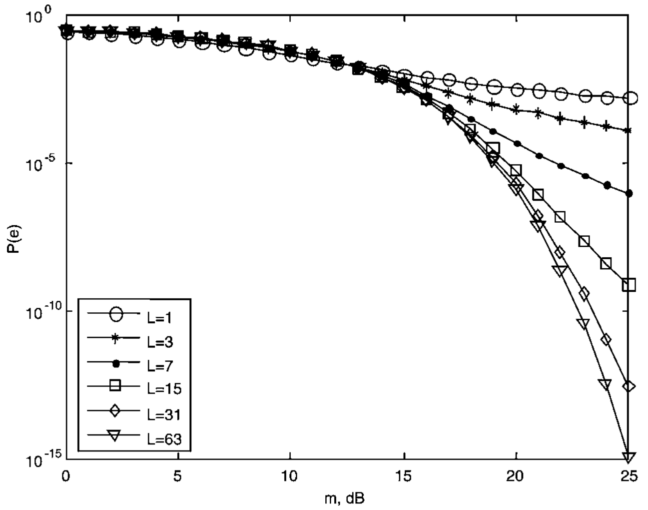

Fig. 7 *Bit error probability with threshold optimisation and majority vote combining for the small phase noise case*

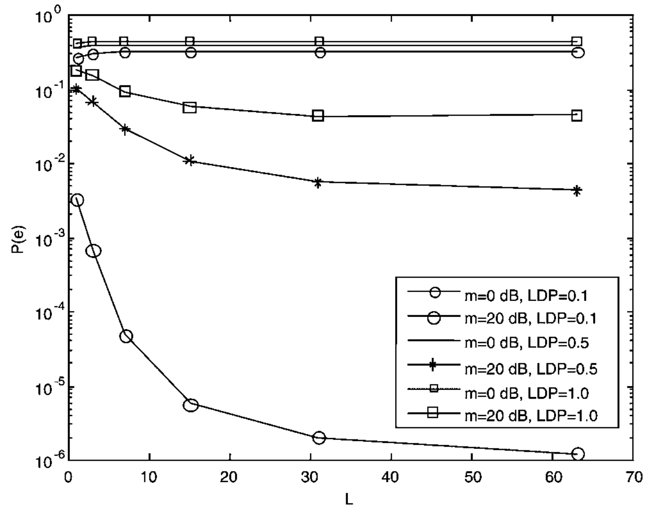

Fig. 9 *Bit error probability as function of the number of chips per bit (LDP = 0.1, 0.5, 1.0)*

5 Receiver complexity issues

The use of symbol slicing, threshold optimisation and majority vote combining have been shown to improve the system performance. This comes at the cost of an increased receiver complexity. A breakdown of the needed additional complexity is as follows (see Fig. 2).

• The variable-limit integrator ($(k-1)T_c$ to kT_c) can be easily realised using a digital integrator with programmable limits. Note that the integration limits are to go through a periodic cycle of variation over the symbol period.
• The variable-threshold comparator can be designed to have a programmable threshold that goes through a periodic cycle of variation over the symbol period. Note that the thresholds are fixed design parameters that are to be pre-calculated (see (28)).
• Chip decisions $\{d_k\}$ can be stored in an L-bit buffer. At the end of a symbol period, a simple logic circuit can perform the majority vote combining operation.

Taking into account the advanced present state of the art in digital circuit technology, the complexity load of the proposed receiver is believed to be acceptable.

6 Conclusions

We have studied the performance of a symbol slicing majority vote combining ASK receiver with phase-noise-optimised decision thresholds. Our results confirm that pure matched filter-based receiver are far from optimum when laser phase noise is present. Decision threshold optimisation and majority vote combining were both shown to be sources of performance improvements.

7 References

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